U.S.S.N. 10,789,527

Claim Amendments

Please amend claims 1, 7-10, 13-17, and 20 as follows:

Please cancel claims 4-6, 11-12, and 18-19 as follows:

Please add new claims 21-24 as follows:

Listing of Claims

1. (currently amended) An embedded semiconductor product comprising:

a semiconductor substrate;

a first isolation trench adjoining a logic cell active region of the semiconductor substrate; and

a second isolation trench adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench;

a first isolation region disposed within the first isolation trench and a second isolation region disposed within the second isolation trench;

wherein a storage capacitor comprising a storage capacitor plate layer at least in part penetrates into the second isolation region.

2. (original) The product of claim 1 wherein the first isolation trench is formed to a depth of from about 2500 to about 5000

angstroms.

3. (original) The product of claim 1 wherein the second isolation trench is formed to a depth of from about 4000 to about 9000 angstroms.

Cancel claims 4-6

7. (currently amended) A method for fabricating an embedded semiconductor product comprising:

providing a semiconductor substrate;

forming a first isolation trench adjoining a logic cell active region of the semiconductor substrate; and

forming a second isolation trench adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench;

forming a first isolation region formed within the first isolation trench and a second isolation region formed within the second isolation trench; and,

forming a storage capacitor comprising a storage capacitor plate layer, said storage capacitor plate layer formed at least in part penetrating into the second isolation region.

8. (currently amended) The method of claim 7 [[1]] wherein the semiconductor substrate is a silicon semiconductor substrate.

9. (currently amended) The method of claim 7 [[1]] wherein the first isolation trench is formed to a depth of from about 2500 to about 5000 angstroms.

10. (currently amended) The method of claim 7 [[1]] wherein the second isolation trench is formed to a depth of from about 5000 to about 6000 angstroms.

Claims 11-12 cancelled

13. (currently amended) The method of claim 7 [[5]] wherein the storage capacitor comprises a sidewall of the second trench, a capacitor dielectric layer formed thereupon and the storage capacitor plate layer formed ~~thereupon~~ on the capacitor

dielectric layer.

14. (currently amended) A method for fabricating an embedded semiconductor product comprising:

providing a semiconductor substrate;

forming simultaneously a first isolation trench adjoining a logic cell active region of the semiconductor substrate and a second isolation trench adjoining a memory cell active region of the semiconductor substrate; ~~and~~

further etching the second isolation trench but not the first isolation trench such that the second isolation trench is deeper than the first isolation trench;

forming a first isolation region formed within the first isolation trench and a second isolation region formed within the second isolation trench; and,

forming a storage capacitor comprising a storage capacitor plate layer, said storage capacitor plate layer formed at least in part penetrating into the second isolation region.

15. (currently amended) The method of claim 14 wherein the semiconductor substrate is a silicon semiconductor substrate.

16. (currently amended) The method of claim 14 wherein the first isolation trench is formed to a depth of from about 2500 to about 5000 angstroms.

17. (currently amended) The method of claim 14 wherein the second isolation trench is formed to a depth of from about 4000 to about 9000 angstroms.

Cancel claims 18-19

20. (currently amended) The method of claim [[5]] 14 wherein the storage capacitor comprises a sidewall of the second isolation trench, a capacitor dielectric layer formed thereupon and the storage capacitor plate layer formed ~~thereupon~~ on the capacitor dielectric layer.

21. (new) The method of claim 20, wherein the capacitor dielectric layer is formed on the logic cell active region to comprise a gate dielectric layer.

22. (new) The method of claim 13, wherein the capacitor dielectric layer is formed on the logic cell active region to comprise a gate dielectric layer.

23. (new) The product of claim 1, wherein the storage capacitor comprises a sidewall of the second isolation trench, a capacitor dielectric layer disposed thereupon and the storage capacitor plate layer disposed on the capacitor dielectric layer.

24. (new) The product of claim 22, wherein the capacitor dielectric layer is disposed on the logic cell active region to comprise a gate dielectric layer.